CLAIMS

What is claimed is:

1. A method comprising:

generating a synchronization clock for sampling signals received by a first device from a memory subsystem and for reducing the number of interface lines between the first device and the memory subsystem, the synchronization clock generated by

selecting a first sampling clock and a second sampling clock so that one clock lies on each side of the midpoint of a calibration data unit, the calibration data unit having transition edges with the midpoint of the calibration data unit centered approximately between with the transition edges, and

interpolating between the first and second sampling clocks to synthesize the synchronization clock, one edge of the synchronization clock located substantially at the midpoint of the calibration data unit.

2. The method of claim 1 further comprising:

generating a plurality of clocks of different phase angles from which the first and second sampling clocks are selected.

3. The method of claim 2 wherein the plurality of clocks have various phase delays ranging from zero to three hundred sixty degrees.

4. The method of claim 2 wherein the plurality of clocks serve to sample the calibration data unit, determine the transition edges of the calibration data unit, and select the first and second sampling clocks, from among the plurality of clocks, to lie within the calibration data unit.

5. The method of claim 2 wherein, from among the plurality of clocks, the two clocks closest to the transition edges of the calibration data unit, but within the calibration data unit, are selected as the first and second sampling clocks.

6. The method of claim 2 wherein, from among the plurality of clocks, the two clocks closest to either side of the calibration data unit midpoint and within the calibration data unit are selected as the first and second sampling clocks.

7. The method of claim 1 wherein interpolating between the first and second sampling clocks includes adjusting the contribution of the first and second sampling clocks to the synthesized synchronization clock to shift one edge of the synchronization clock to lie substantially at the midpoint of the calibration data unit.

8. The method of claim 1 wherein the synchronization clock and calibration data unit each include a leading transition edge, the leading transition edge of the synchronization clock is ninety degrees delayed from the leading transition edge of the calibration data unit.

9. A machine-readable medium having one or more instructions to generate a synchronization clock to sample an incoming synchronous data stream and reduce the number of interface lines between a first device and a memory subsystem, which when executed by a processor, causes the processor to perform operations comprising:

selecting a first sampling clock and a second sampling clock with one clock on each side of the midpoint of a calibration data unit, the calibration data unit having transition edges with the midpoint of the calibration data unit centered approximately between with the transition edges; and

interpolating between the first and second sampling clocks to synthesize the synchronization clock, one edge of the synchronization clock located substantially at the midpoint of the calibration data unit.

10. The machine-readable medium of claim 9 further comprising:

generating a plurality of clocks of different phase angles from which the first and second sampling clocks are selected.

11. The machine-readable medium of claim 10 wherein the plurality of clocks have various phase delays ranging from zero to three hundred sixty degrees.

12. The machine-readable medium of claim 10 wherein the plurality of clocks serve to sample the calibration data unit, determine the transition edges of the calibration data unit, and select the first and second sampling clocks, from among the plurality of clocks, to lie within the calibration data unit.

13. The machine-readable medium of claim 10 wherein, from among the plurality of clocks, the two clocks closest to the transition edges of the calibration data unit but within the calibration data unit are selected as the first and second sampling clocks.

14. The machine-readable medium of claim 10 wherein, from among the plurality of clocks, the two clocks closest to either side of the calibration data unit midpoint and within the calibration data unit are selected as the first and second sampling clocks.

15. The machine-readable medium of claim 9 wherein interpolating between the first and second sampling clocks includes adjusting the contribution of the first and second sampling clocks to the synthesized synchronization clock to shift one edge of the synchronization clock to lie substantially at the midpoint of the calibration data unit.

16. The machine-readable medium of claim 15 wherein the synchronization clock includes a leading edge, the leading edge of the synchronization clock is ninety degrees delayed from the leading edge of the calibration data unit.

17. An apparatus comprising:

a receiver interface with one or more inputs to receive one or more data streams; and

a clock synthesizer coupled to the receiver interface to generate an internal synchronization clock for sampling a received data stream, the clock synthesizer to generate the internal synchronization clock by detecting transition edges of a calibration data pattern.

18. The apparatus of claim 17 wherein the clock synthesizer includes,

a clock generator to generate a plurality of sampling clocks,

an edge detector coupled to the clock generator, the edge detector configured to sample the calibration data pattern using at least two of the sampling clocks and detect transition edges of the calibration data pattern, and

a controller coupled to the edge detector, the controller configured to select a first and second sampling clocks from among the at least two sampling clocks and interpolate between the first and second sampling clocks to synthesize the internal synchronization clock.

19. The apparatus of claim 18 wherein the plurality of sampling clocks are of different phase angles.

20. The apparatus of claim 18 wherein the plurality of clocks are phase delayed from zero to three hundred sixty degrees.

21. The apparatus of claim 18 wherein the calibration data pattern includes at least one calibration data unit, the calibration data unit being defined by two transition edges, the plurality of clocks serve to sample one calibration data unit of the calibration data pattern, the edge detector is configured to determine the location of the transition edges of the calibration data unit, and the controller is configured to select the first and second sampling clocks to lie within the calibration data unit.

22. The apparatus of claim 21 wherein the controller is configured to select from among the plurality of clocks the two clocks closest to the transition edges of the calibration data unit but within the transition edges of the calibration data unit as the first and second sampling clocks.

23. The apparatus of claim 21 wherein the controller is configured to select from among the plurality of clocks the two clocks closest to either side of the calibration data unit midpoint, between the transition edges, and within the transition edges of the calibration data unit as the first and second sampling clocks.

24. The apparatus of claim 18 wherein interpolating between the first and second sampling clocks the controller is configured to adjust the contribution of the first and second sampling clocks to the synthesized internal synchronization clock to shift one edge of the clock to lie substantially at

the midpoint between the transition edges of the calibration data unit.

25. The apparatus of claim 18 wherein the internal synchronization clock and calibration data unit each have a leading transition edge, the leading transition edge of the internal synchronization clock is ninety degrees delayed from the leading transition edge of the calibration data unit.

26. A system comprising:

a memory subsystem to store data;

a first device communicatively coupled to the memory subsystem to receive a data stream from the memory subsystem, the first device including

a clock synthesizer to generate an internal synchronization clock for sampling the data stream by detecting transition edges of a calibration data pattern transmitted by the memory subsystem.

27. The system of claim 25 wherein the clock synthesizer includes,

a clock generator to generate a plurality of sampling clocks,

an edge detector coupled to the clock generator, the edge detector configured to sample the calibration data pattern using at least two of the sampling clocks and detect transition edges of the calibration data pattern, and

a controller coupled to the edge detector, the controller configured to select a first and second sampling clocks from among the at least two sampling clocks and interpolate between the first and second sampling clocks to synthesize synchronization clock for sampling data streams.

28. The apparatus of claim 27 wherein the calibration data pattern includes at least one calibration data unit, the

calibration data unit being defined by two transition edges, the plurality of clocks serve to sample one calibration data unit of the calibration data pattern, the edge detector is configured to determine the location of the transition edges of the calibration data unit, and the controller is configured to select the first and second sampling clocks to lie within the calibration data unit.

29. The apparatus of claim 27 wherein the controller is configured to select from among the plurality of clocks the two clocks closest to the transition edges of the calibration data unit but within the transition edges of the calibration data unit as the first and second sampling clocks.

30. The apparatus of claim 27 wherein interpolating between the first and second sampling clocks the controller is configured to adjust the contribution of the first and second sampling clocks to the synthesized internal synchronization clock to shift one edge of the clock to lie substantially at the midpoint between the transition edges of the calibration data unit.